A breadboard for real-time image processing on board Gaia

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Outline

I. Gaia

user requirements

II. Image analysis

algorithmic framework

III. VHDL pipeline

the logic behind the scenes

IV. The demonstrator: a case study

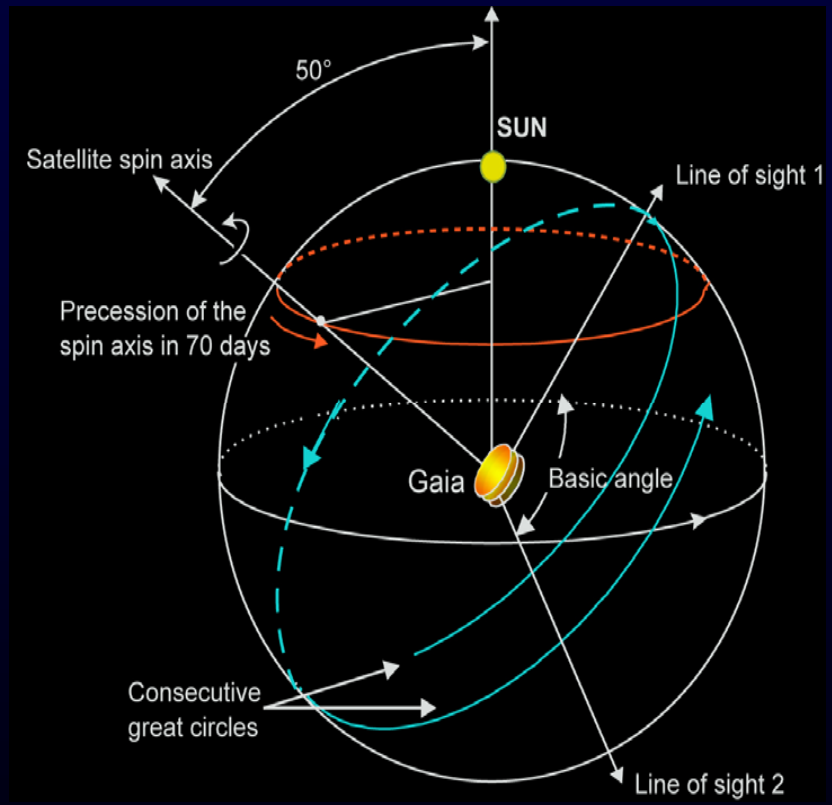
some solutions to some problems

V. Conclusion

I. Gaia

Observing principle

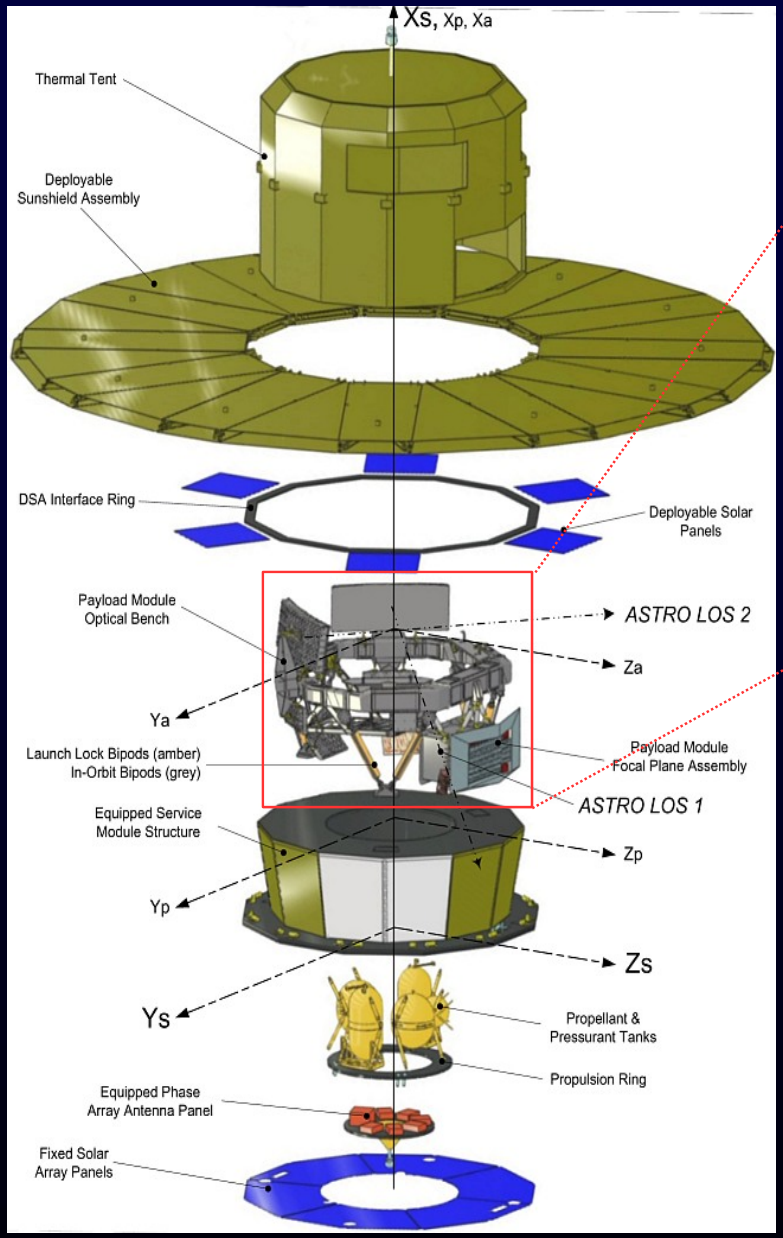
- Global astrometry survey
  - **2 telescopes with combined focal planes**
  - **spin & precession motions**
    - **→ on-the-fly data acquisition**
    - **→ attitude & orbit control**
  - **106 CCDs & L2 orbit**
    - **→ selective data acquisition**
    - **→ autonomous data management**
  - **survey: no star catalogue selection biases**
    - **→ on-board object detection**

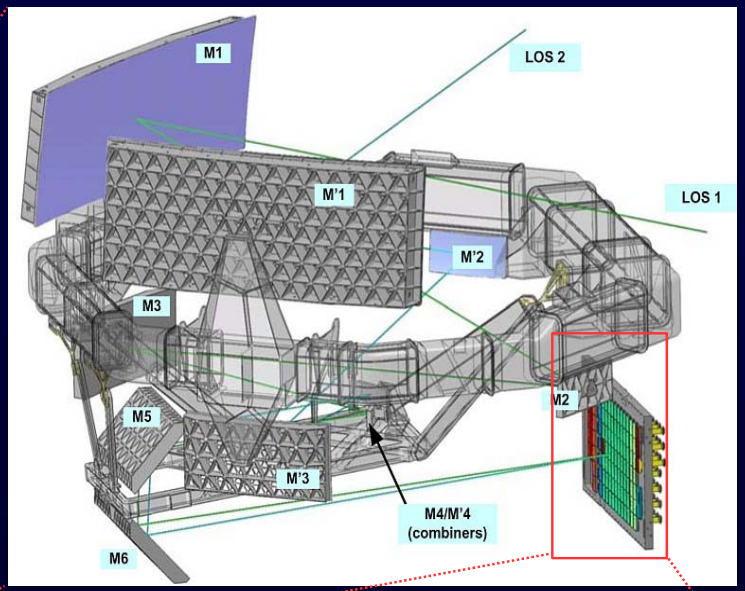


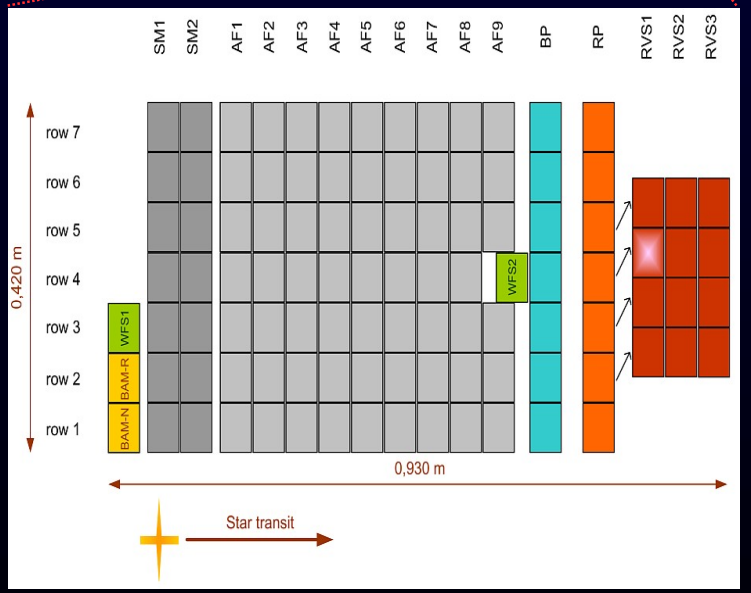
Gaia

Payload

Gaia

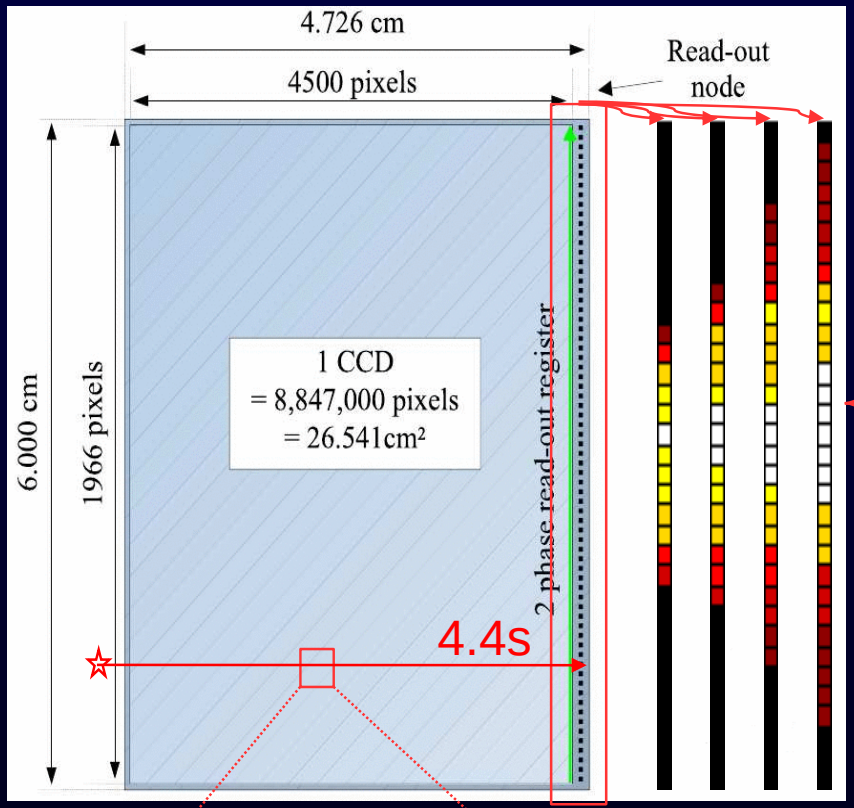




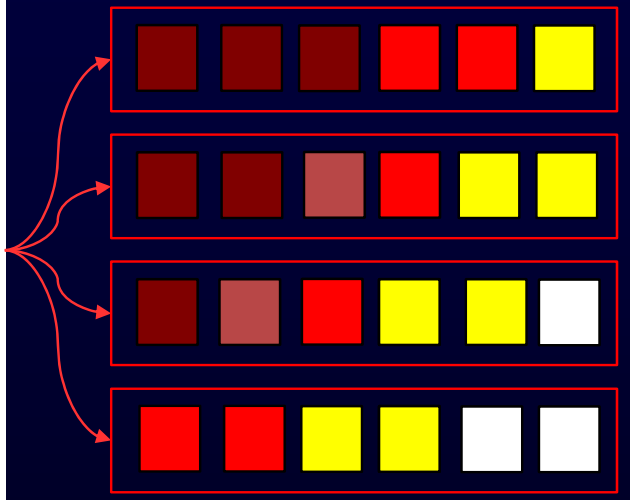


Time-delay integration (TDI)

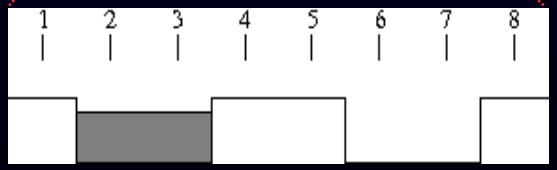
Gaia



column per column read-out
(every 0.9828 ms)



pixel packets sent to
Video Processing Unit
(SpaceWire interface)

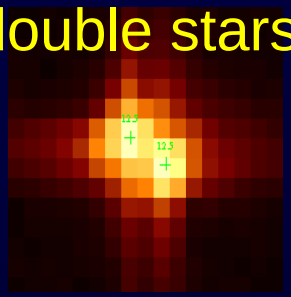


4 phase charge transfer

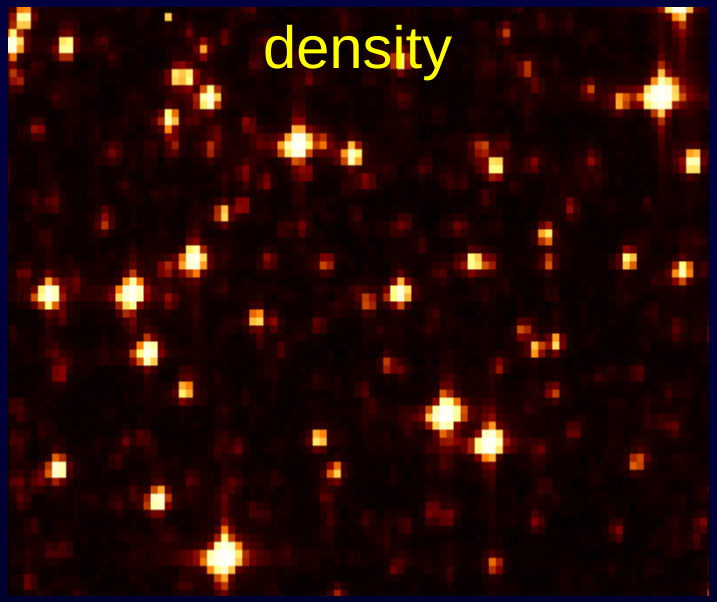
Some cases of interest

Gaia

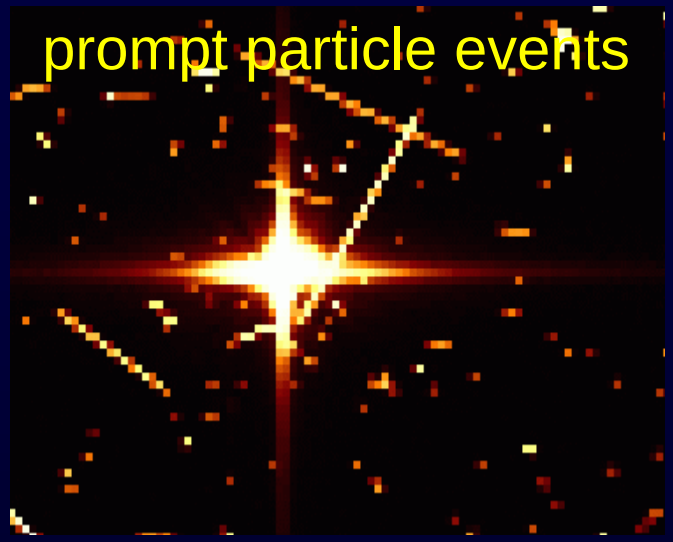
double stars



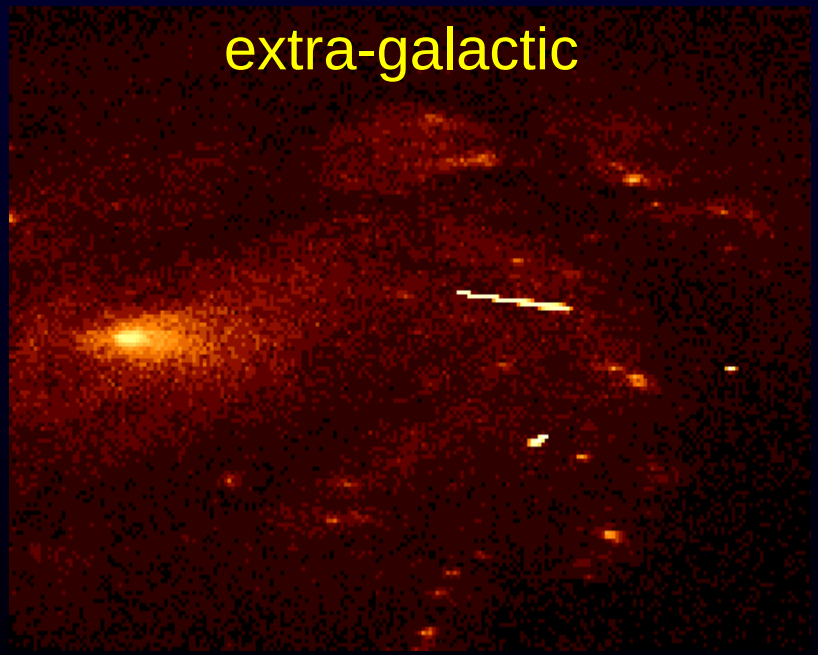
density



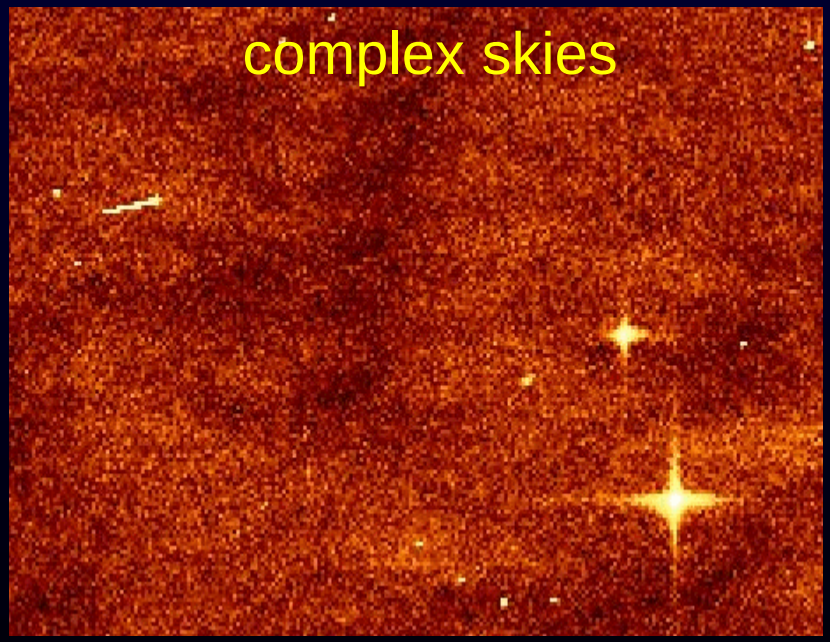
prompt particle events



extra-galactic



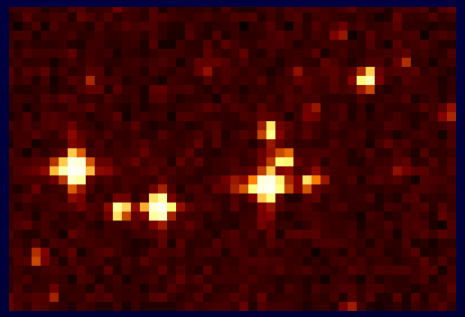
complex skies



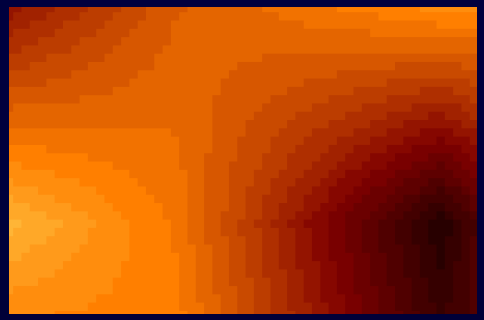
II. Image analysis

Functional architecture

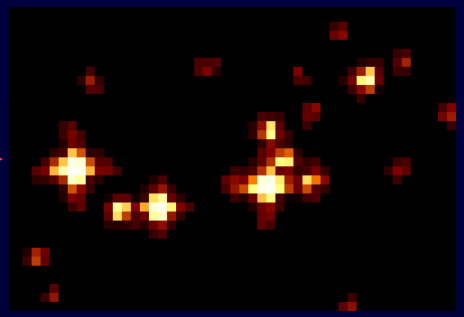
Image analysis



raw data

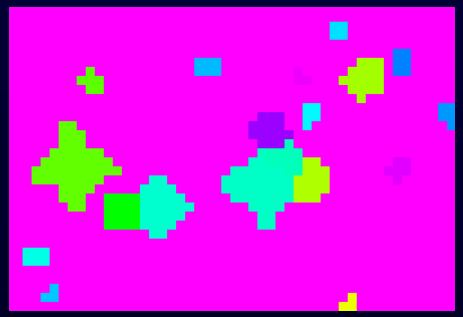


background map

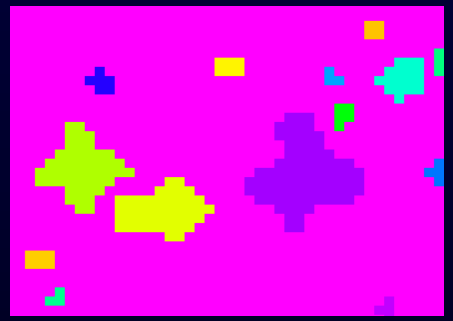


thresholded

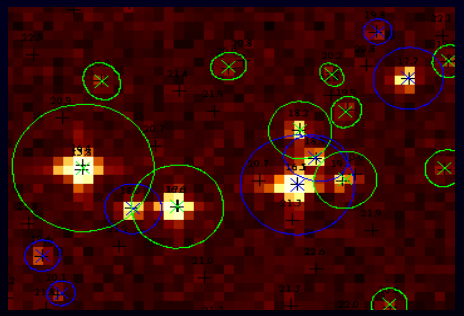
pixel level



segmentation



connected components

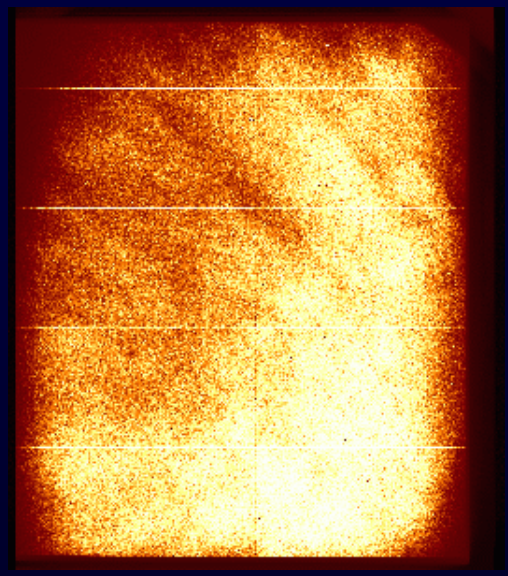


measurements

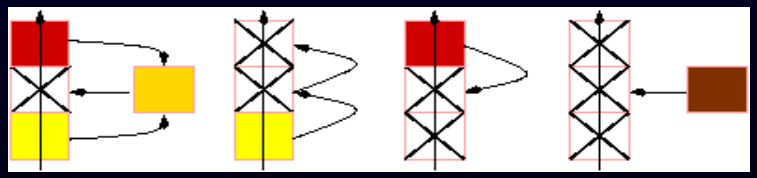
object level

Pre-calibration

- Needs
  - **control the selection function**
  - **avoid false detections**
  - **graceful degradation of performance in time**
- Method
  - **linear transform (generalises flat-field & dark)**
  - **replacement mechanism**
  - **fixed-point arithmetics**



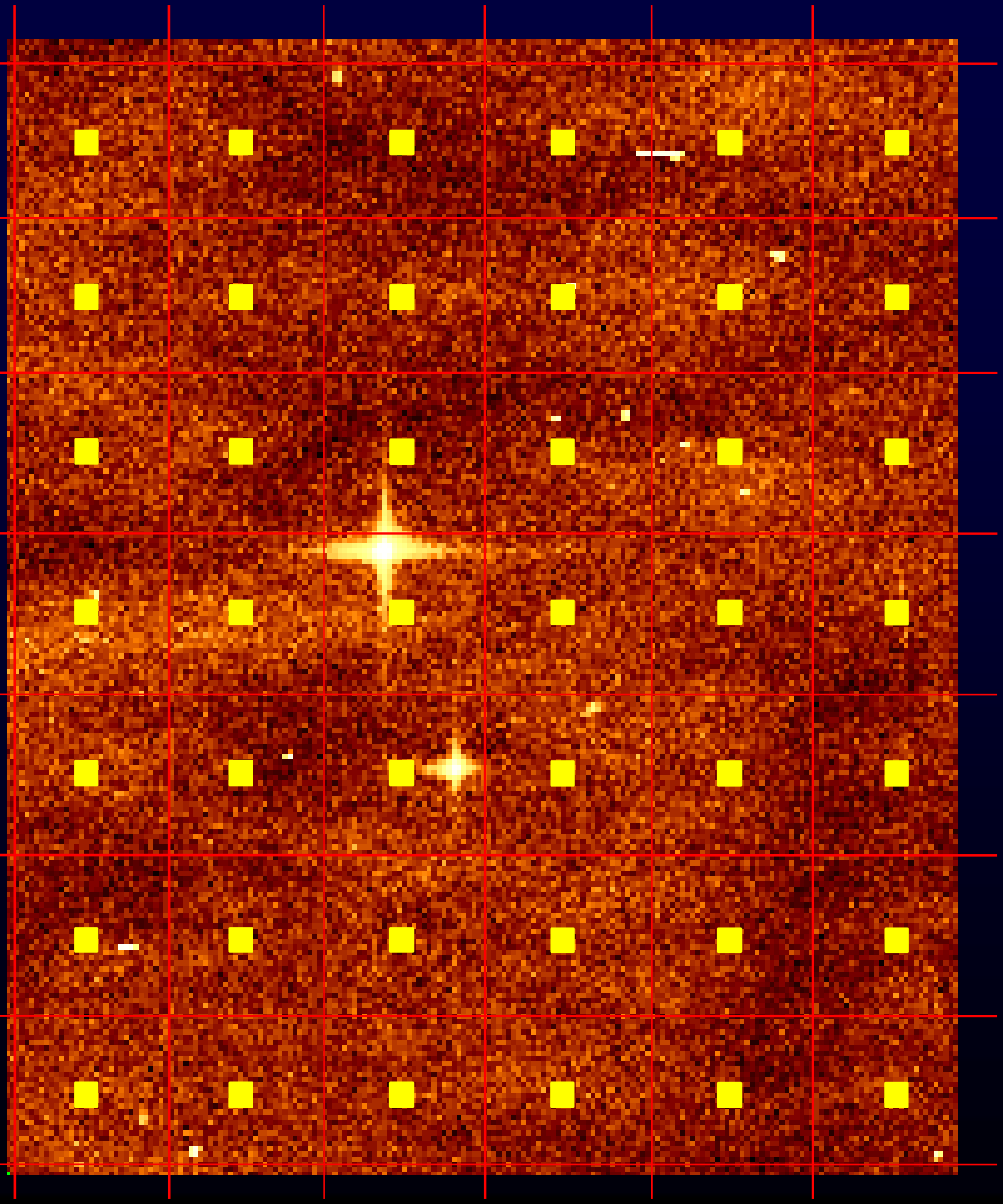
(VIMOS CCD)



Background

- Needs
  - **control the selection function: estimate the total noise**
  - **control false detections**
- Functional
  - **latency & resolution trade-off**
  - **robust to stellar content**
  - **systematic calculation**
- Method
  - **regional estimates: hyperpixels**
  - **histograms: 4 ADU bins**
  - **interpolated mode: precise & robust**
  - **2D bilinear interpolation**
  - **fixed-point arithmetics**

Background II (1)

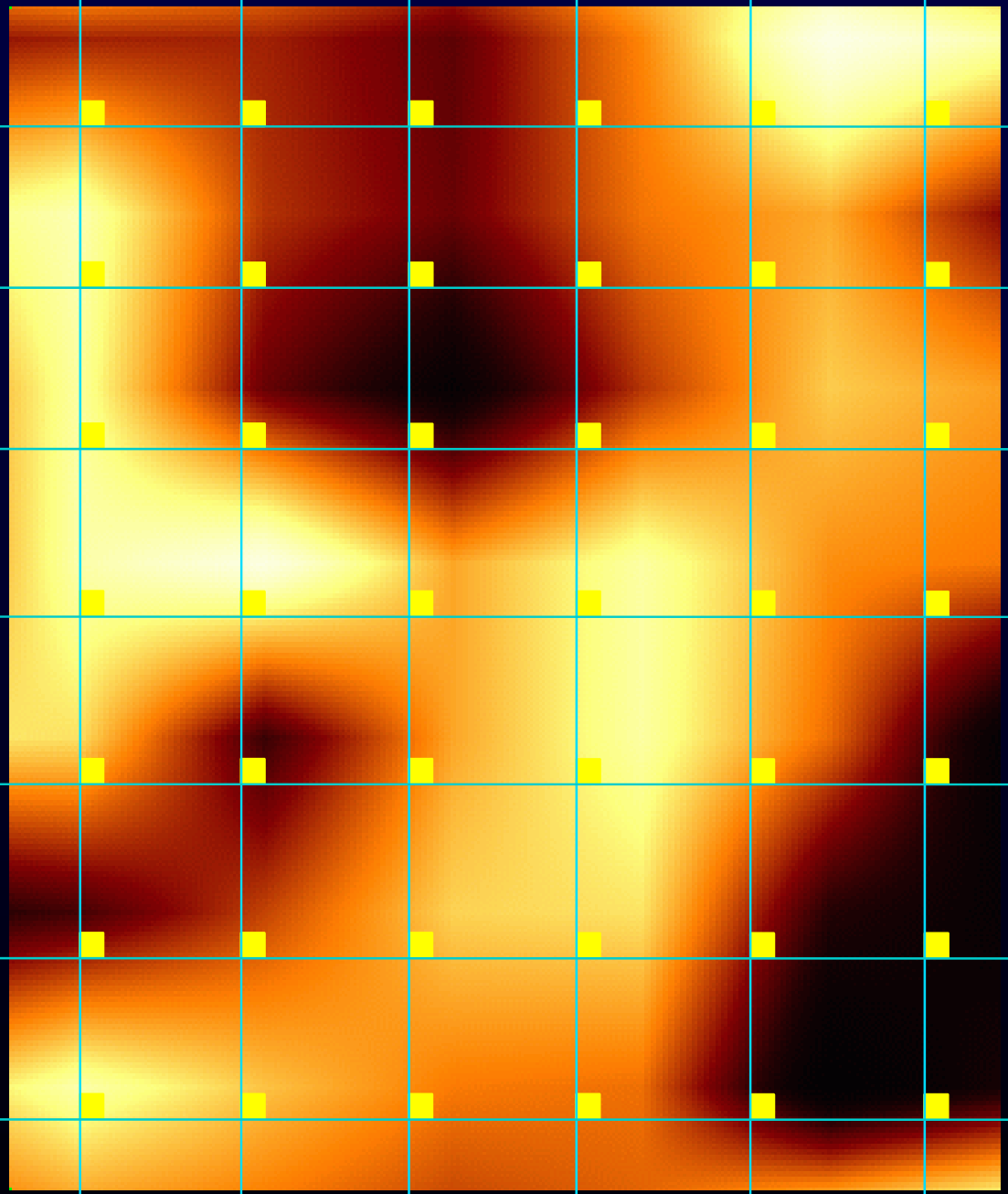


hyperpixel

mode values

Image analysis

Background II (2)

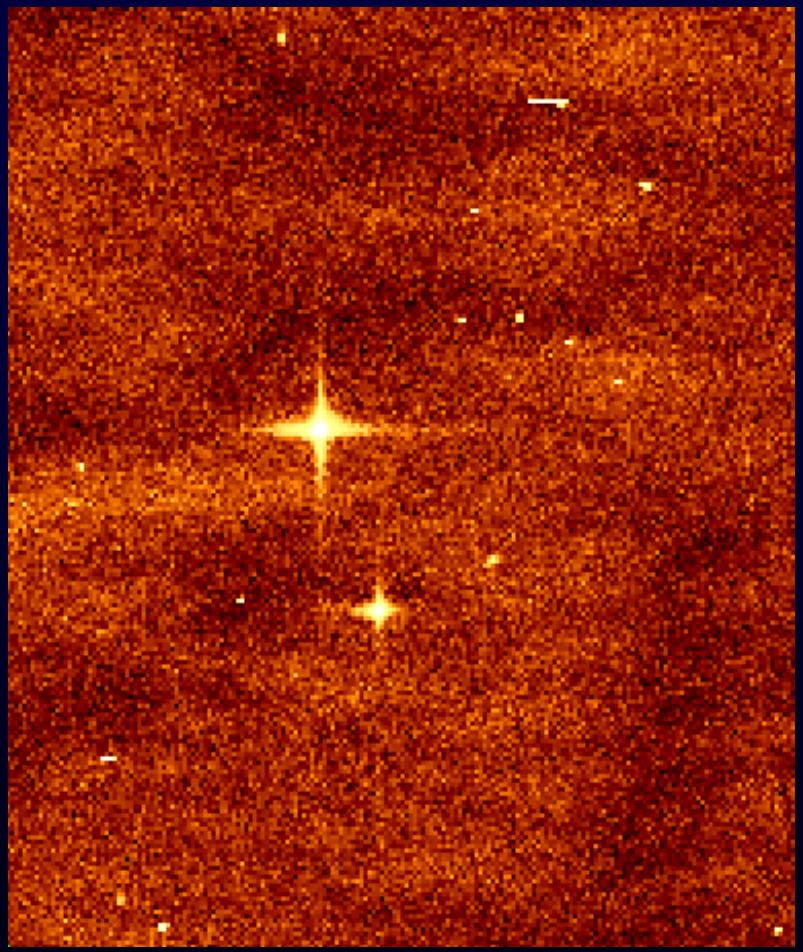


mode values

interpolation

Image analysis

Background II (3)



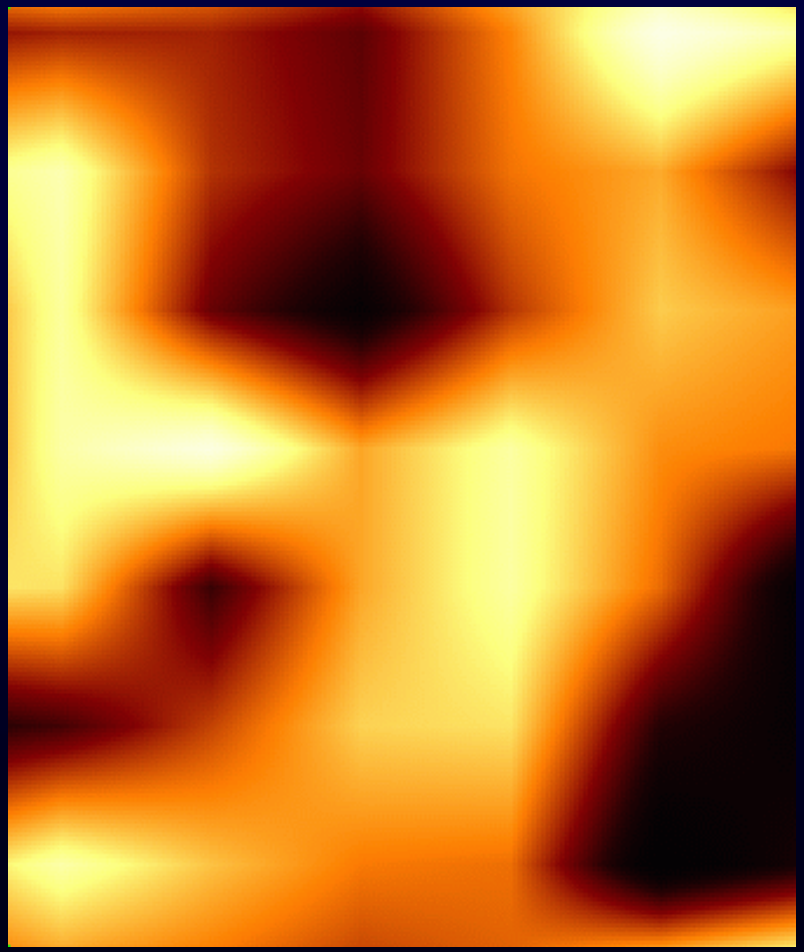


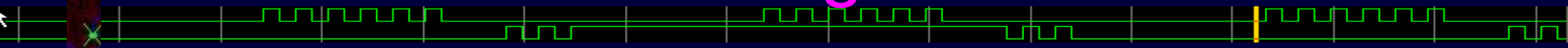
Image analysis

Pixel selection

- Needs
  - **save resources**
    - **→ discard background pixels**
  - **control false detections**
    - **→ robustness to noise**
    - **→ filter faint stars**
- Method
  - **signal to noise threshold**
  - **signal: subtract estimated background**
  - **fixed-point arithmetics**

III. VHDL pipeline

Design



VHDL pipeline

- Pipeline
  - **pre-calibration → buffer_pix → background → pixel selection**
  - **data driven & exploiting the available latency**
  - **target slow operation (timing constraints, power consumption, resource sharing)**
- Clocks
  - **DCLK: data clock → pipeline control (~1 MHz)**
  - **SCLK: SRAM clock → sequential optimisations (~32 MHz)**
  - **CLK: main clock → SRAM interface (125 MHz)**
- Design for test
  - **interchangeable processing core & debug core**
  - **conditional instantiation → modular for unit validation**
    → increasing complexity

Pixel selection (1)

- Tasks
  - **on demand background interpolation** → **optimise storage**
  - **signal to noise threshold** → **fixed-point arithmetics**
  - **output stream of selected pixels** → **~90% data reduction prior to software**

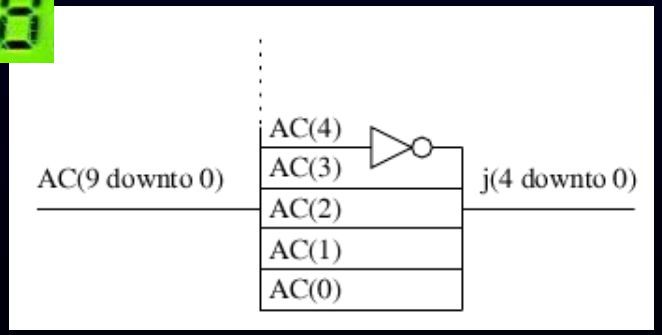
- Pipeline

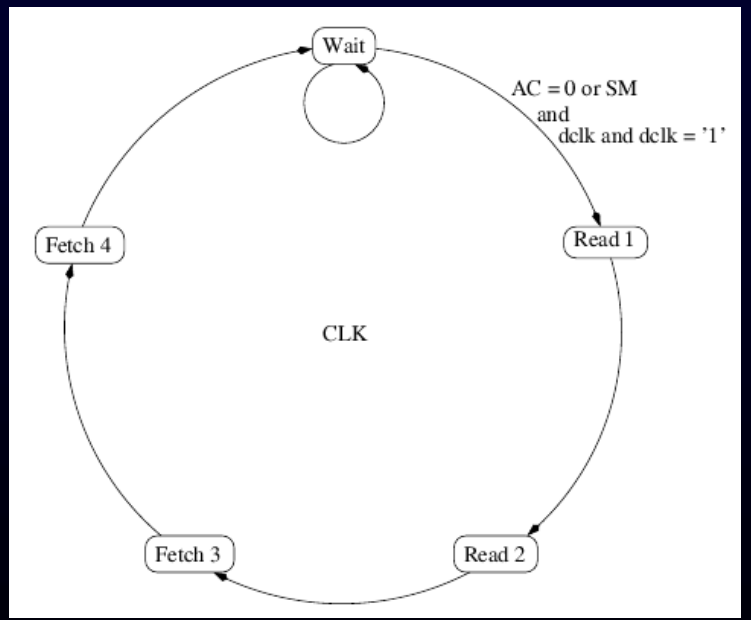
DCLK

VHDL pipeline

mode addresses (x4)
AL & AC coordinates

interpolation coefficients
read modes (x4)





Pixel selection (2)

- Tasks
  - on demand background interpolation → optimise storage
  - signal to noise threshold → fixed-point arithmetics
  - output stream of selected pixels → ~90% data reduction prior to software

- Pipeline

mode addresses (x4)
AL & AC coordinates

signal

interpolation coefficients
read modes (x4)

signal^2
threshold

contributions (x4)

test
output

sum

$$\underbrace{mode_{0,0}}_{0.11.11} \times 2^{10} - mode_{0,0} \underbrace{(i+j)}_{0.0.6} \times 2^5 + mode_{0,0} \times \underbrace{i \times j}_{0.0.10} + \dots$$

VHDL pipeline

Synthesis (1)

- VHDL
  - **ESA standard (except for testing: verification & validation)**

VHDL pipeline

I if:

$$\overline{WE}^1_{LZWE}.(\quad \overline{WE}^0_{OHA}.(\overbrace{A^0_{OHA}.\overline{WE}^0}^{4} + \overbrace{A^1_{OHA}.\overline{WE}^1.A^0_{AA}}^{20})$$

$$+\overline{WE}^1_{OHA}.(A^1_{AA}.(\overbrace{\overline{WE}^0_{HZWE}.\overline{WE}^0}^{9} + \overbrace{\overline{WE}^0_{RC}.\overline{WE}^1}^{24\ 27})$$

$$+ A^0_{AA}.(\overline{WE}^0.(\overbrace{A^0_{OHA}}^{7\ 10\ 13} + A^1_{OHA}.(\overbrace{\overline{WE}^0_{HZWE}}^{8} + \overbrace{\overline{WE}^1_{RC}}^{14}) + \overbrace{\overline{WE}^1.A^1_{OHA}}^{23\ 26\ 29}))))$$

II if:

$$\overline{WE}^0.(\overbrace{\overline{WE}^0_{LZWE}.A^0_{OHA}}^{1} + \overbrace{\overline{WE}^0_{OHA}.A^1_{OHA}}^{2\ 3\ 5\ 6}) + \overline{WE}^1.\overline{WE}^1_{RC}.(\overbrace{A^0_{OHA}}^{28} + \overbrace{A^1_{AA}}^{30})$$

III if:

$$\overbrace{\overline{WE}^1_{RC}.\overline{WE}^0.A^1_{AA}}^{15}$$

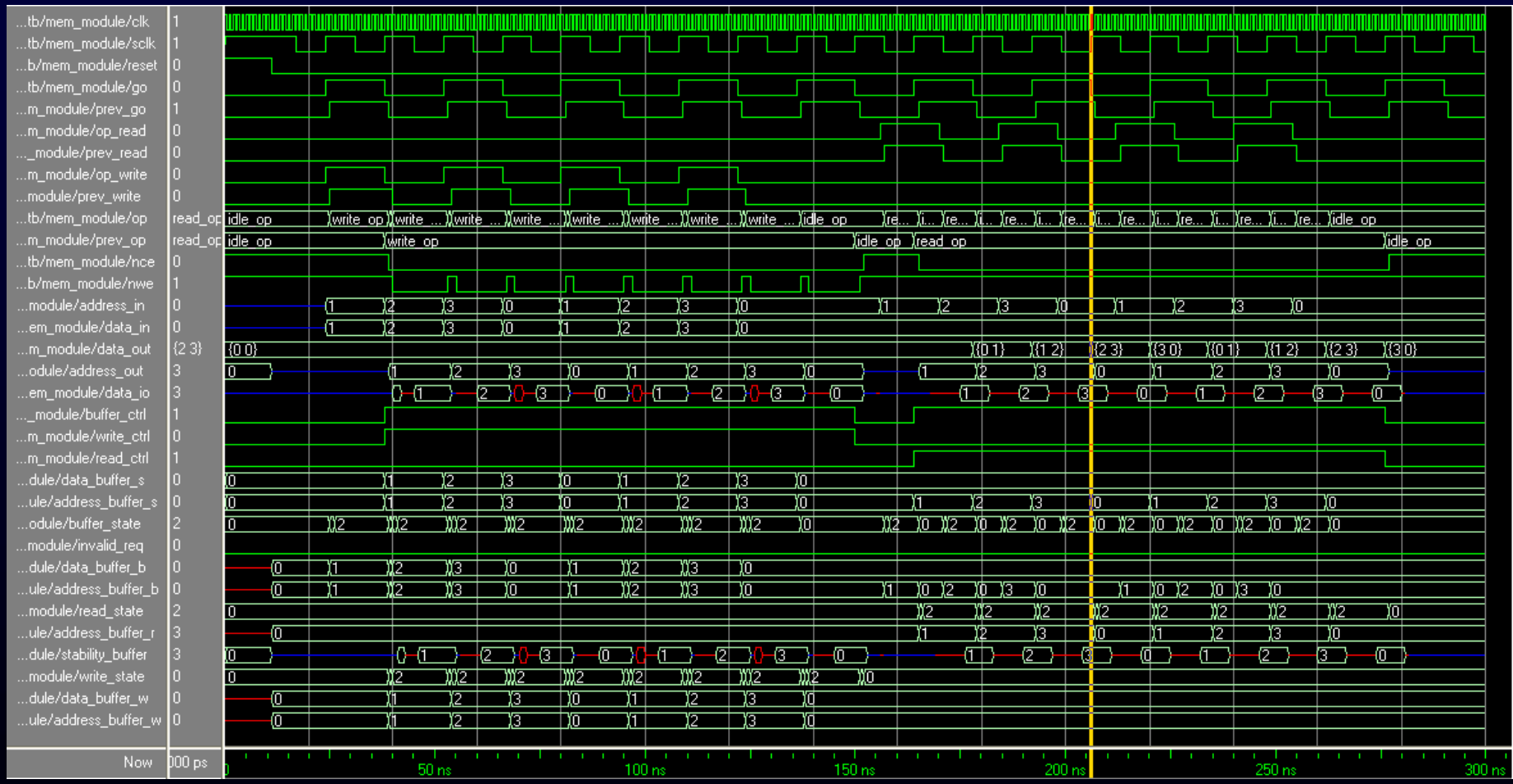
$$+\overline{WE}^0_{RC}.(\quad \overline{WE}^1_{HZWE}.(\overbrace{A^1_{AA}.\overline{WE}^0}^{12} + \overbrace{A^0_{OHA}.\overline{WE}^1}^{25} + \overbrace{A^1_{OHA}.\overline{WE}^0}^{11})$$

$$+\overline{WE}^0_{HZWE}.(\overbrace{\overline{WE}^1_{OHA}.\overline{WE}^1.A^0_{OHA}}^{22}$$

$$+ \overline{WE}^0_{OHA}.\overline{WE}^1.(\overbrace{\overline{WE}^0_{LZWE}}^{16\ 17\ 18} + \overline{WE}^1_{LZWE}.(\overbrace{A^0_{OHA}}^{19} + \overbrace{A^1_{AA}}^{21}))))$$

Synthesis (2)

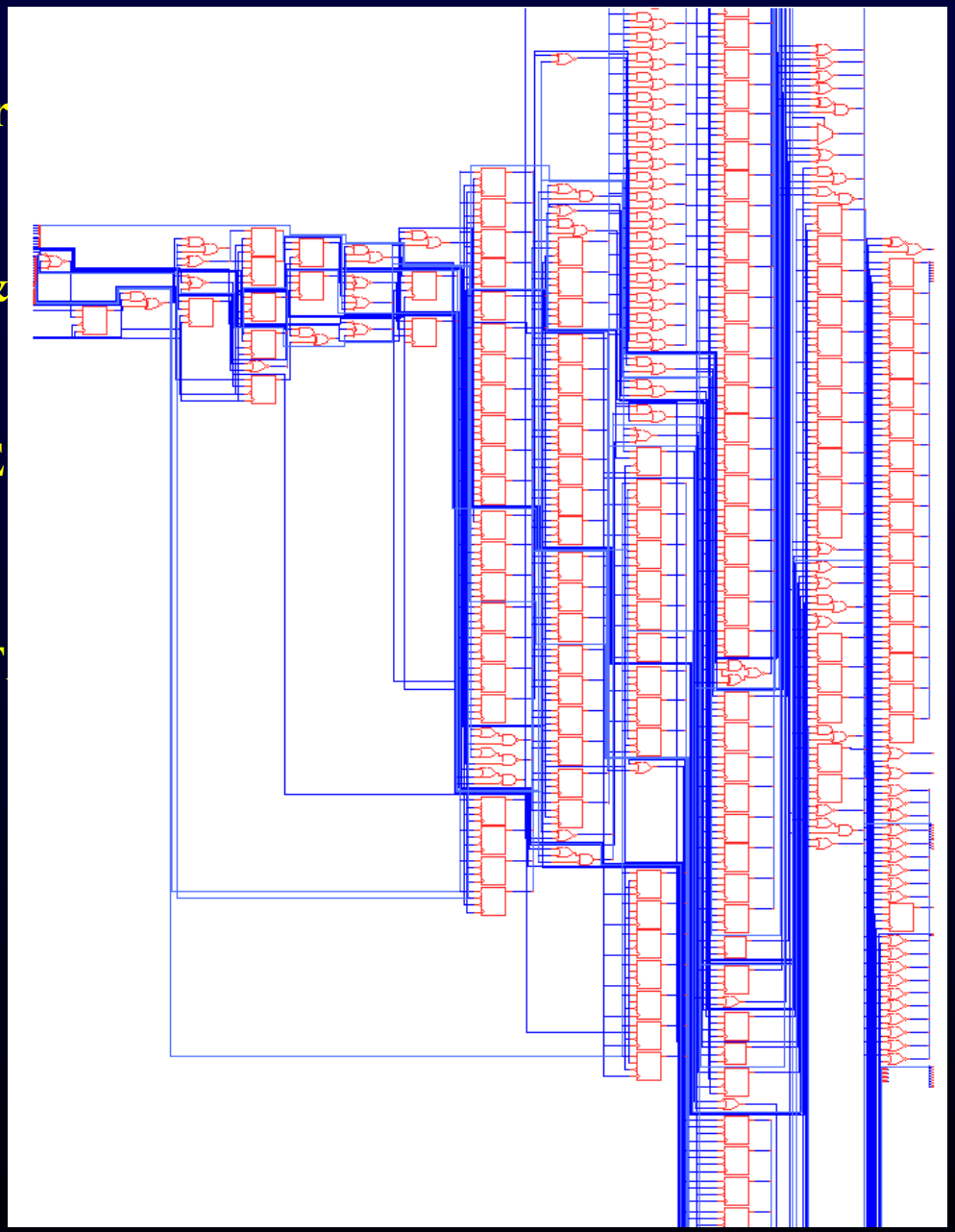
- VHDL
  - **ESA standard (except for testing: verification & validation)**
- Simulation



VHDL pipeline

Synthesis (3)

- VHDL
  - **ESA standard (except for**
- Simulation
  - **validated pre-synthesis &**
- Synthesis
  - **14722 cells > ProASIC3E margin)**
  - **slow routing**
  - **target: RTAX-S 1000 (IT**



Synthesis (4)

- VHDL
  - **ESA standard (except for testing: verification & validation)**
- Simulation
  - **validated pre-synthesis & post-synthesis**
- Synthesis
  - **14722 cells > ProASIC3E 600 → ProASIC3E 1500 (100% margin)**
  - **slow routing**
  - **target: RTAX-S 1000 (ITAR)**

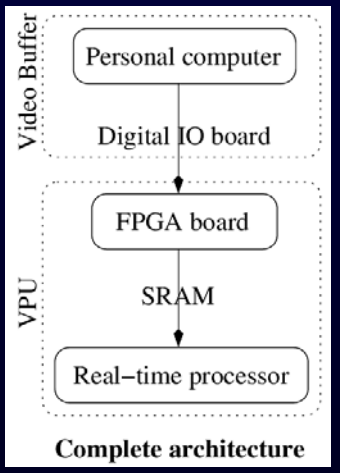
Architecture		Processing core	
Component	Cells	Component	Cells
Framework	137	General	106
Handshake manager	329	Scheduler	327
Debug core	233	Precalibration	1844
Processing core	11970	Buffering	210
Controllers	2×599	Histogram	4140
Switch	137	Mode	1533
CLK division	35	Pixsel	3900
Total	14722		11970

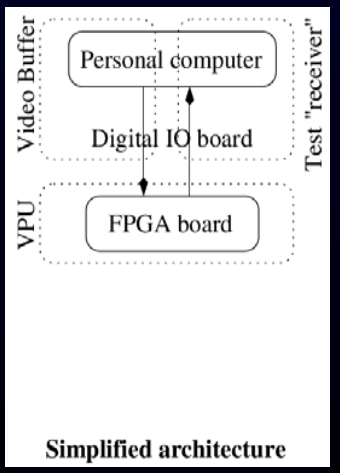
IV. The demonstrator: a case study

Architecture

- Interfaces
  - input: CCDs via serial SpaceWire link
    → video buffer: PC with IO board (handshake)
  - output → hard/soft interface: dual-port asynchronous SRAM
  - storage → 2 asynchronous SRAMs

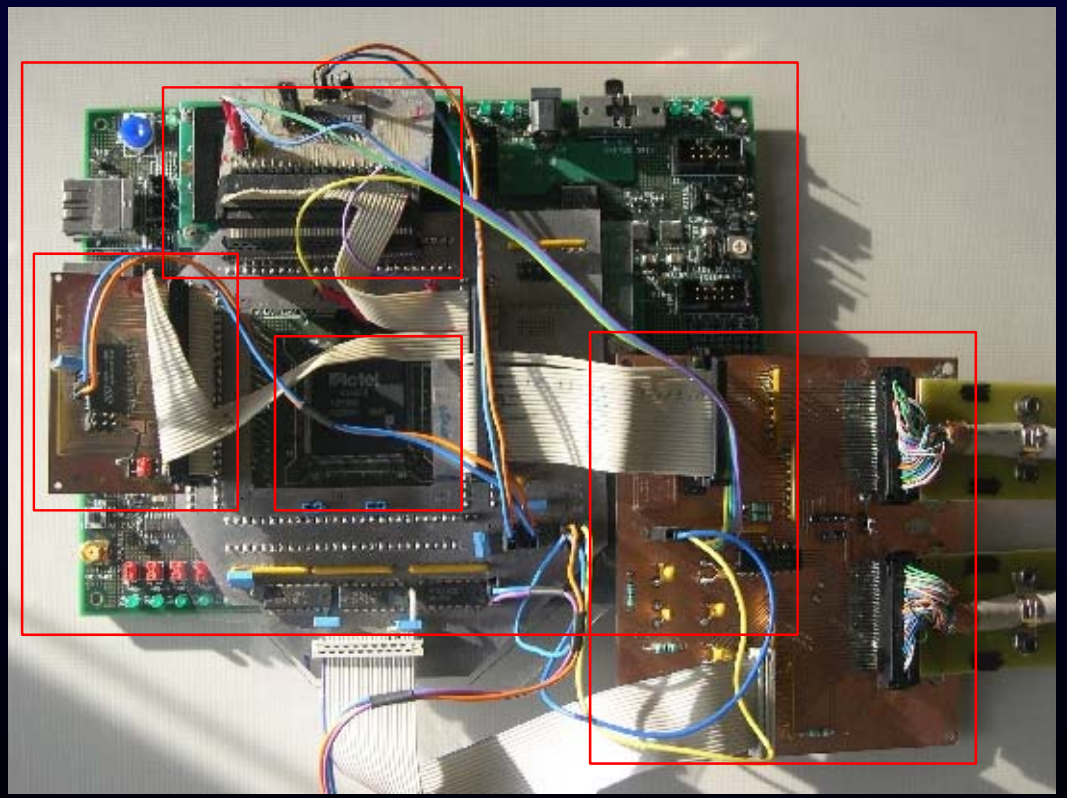
- Simplified
  - FPGA board developments
    → no real-time processor
  - design simplifications
    → no connected component labelling
    → no management of software interface
  - inspectable design
    → conditional module instantiation
    → output data stored in PC
    → free pins





Platform

- Part
  - **Actel: ProASIC3E instead of RTAX-S**
    - **→ reprogrammable: flash-based instead of anti-fuse**
    - **→ slower (interconnections)**
    - **→ less dense**
- Development Kit
  - **ProASIC3E 600**
- SRAMs
  - **ISSI ISI61LV51216**
  - **static**
  - **asynchronous**
  - **16-bit data**
  - **19-bit address**
- PC interface
  - **handshake**
  - **16-bit data**



IOs: Experimental observation

- Logic
  - **protocol timing failures: need to adjust timing to IO board**
  - **idle cycles: disrupted logic**
- Analogic
  - **noise**
  - **glitches**
  - **overshoots**
  - **ground noise**

→ Functional for 60% of the maximum load (16 SSOs)

Signal integrity problems

- Fast transitions (~1 ns)
  - **current rush**
  - **harmonics**
- Impedance issues
  - **inadequate line transmission**
  - **improper routing (common impedances, long paths)**
- Power supply design
  - **poor ground reference**
  - **ineffective decoupling**
  - **multiple power supplies**

Solutions

- IO characteristics & routing
  - **driver's strength reduced**
  - **driver's capacitance increased**
  - **schmitt triggers added on inputs**
  - **insertion of strong quiet outputs between sensitive signals**
  - **delay buffers to avoid SSO**

- Boards modified
  - **impedance** → **line terminations when possible**
    → **diversion of the current paths**
  - **power supply** → **passive solutions preferred (terminations & level adaptation)**
    → **kept one power supply only**
    → **improvement of ground routing**
    → **decoupling capacitors**
    → **use of ferrite beads**

→ **Functional at the maximum load (occasional perturbations)**

V. Conclusion

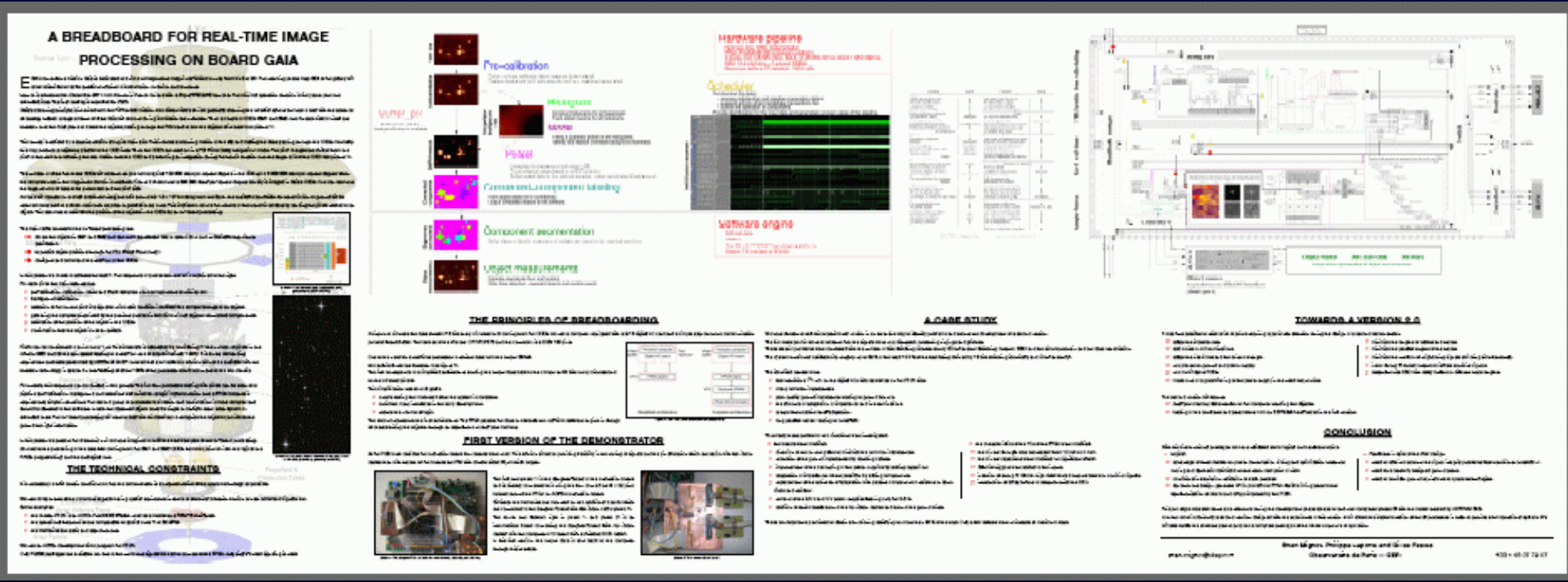
Conclusion

- Science
  - designed in collaboration with scientists
  - satisfactory: completeness, false detection rate, special objects (binary stars, textured backgrounds etc.)
- Feasibility
  - meets user requirements & system-level constraints (data flow)
  - representative demonstrator (technology & logic): portable to RTAX
  - multiple clock synchronous design: data driven timing, relaxed constraints, power consumption
  - test platform for testing & validation (& improvement !)
- Lessons learnt
  - logic design: resource sharing, scheduling, fixed-point arithmetics etc.
  - signal integrity is a key issue (even for slow designs due to transitions)
  - need for careful design of the ground reference !

Perspectives

- Towards a 2nd demonstrator
  - **improvements**
    - **multi-layer PCB**
    - **compact design**
    - **power supply design**
    - **impedances**
  - **extensions**
    - **interface to software: dual-port asynchronous SRAM**
    - **EEPROM & initialisation**
    - **real-time software engine (PPC750FX)**
- Testing & validation
  - **ECSS: verification (correctness) & validation (intended use)**
  - **compare to industrial system (Astrium SAS)**

More details, discussion etc.



Poster !